Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A reprogrammable fuse apparatus, comprising:

a plurality of rewriteable electronic fuses, each having a nonvolatile memory element, arrayed in a predetermined configuration; and

a plurality of high-voltage switches, each high-voltage switch corresponding to an associated electronic fuse of said plurality of electronic fuses, and each high-voltage switch having a high-voltage input terminal and a fuse-state state-setting input terminal,

wherein a given electronic fuse of the plurality of electronic fuses is programmed by selecting and coupling an associated control signal to the given electronic fuse.

2. (Original) The electronic fuse array of Claim 1, wherein each electronic fuse comprises a CMOS latch having two cross-coupled inverters.

3. (Original) The electronic fuse array of Claim 1, wherein the nonvolatile memory element of each electronic fuse comprises a floating-gate transistor having a floating gate, an amount of charge on the floating gate of any given nonvolatile memory element determining a memory value of the given nonvolatile memory element.

4. (Original) The electronic fuse array of Claim 3, wherein each nonvolatile memory element includes a first capacitor, each first capacitor of any given nonvolatile memory

element having a first plate in common with the floating gate of the floating-gate transistor of the given nonvolatile memory element.

5. (Original) The electronic fuse array of Claim 1, wherein the nonvolatile memory elements are manufactured in a standard CMOS fabrication process.

6. (Original) The electronic fuse array of Claim 3, wherein each floating-gate transistor of each electronic fuse is a transistor selected from the group consisting of: nFET, pFET, FinFET, and multi-gate FET.

7. (Original) The electronic fuse array of Claim 1, wherein said nonvolatile memory element of each electronic fuse is a memory element using a mechanism selected from the group consisting of magnetoresistive , ferroelectric, phase-change, and dielectric, for nonvolatile storage of information.

8. (Original) The electronic fuse array of Claim 3, of any given floating-gate transistor wherein the amount of charge on a floating gate may be changed using Fowler-Nordheim tunneling.

9. (Original) The electronic fuse array of Claim 3, wherein the amount of charge on a floating gate may be changed using hot-electron injection.

10. (Original) The electronic fuse array of Claim 3, wherein the amount of charge on a floating gate may be changed using direct tunneling.

11. (Original) The electronic fuse array of Claim 3, wherein the amount of charge on a floating gate may be changed using hot-hole injection.

12. (Original) The electronic fuse array of Claim 3, wherein the amount of charge on a floating gate may be changed using ultraviolet radiation exposure.

13. (Original) The electronic fuse array of Claim 4, wherein each nonvolatile memory element further includes a second capacitor, each second capacitor of any given nonvolatile memory element having a first plate in common with the floating gate of the floating-gate transistor of the given nonvolatile memory element.

14. (Original) The electronic fuse array of Claim 2, wherein each electronic fuse has a capacitive element coupled to an output of its latch.

15. (Original) The electronic fuse array of Claim 13, wherein a second plate of the first capacitor in each electronic fuse is coupled to a first output of an associated high-voltage switch and a second plate of the second capacitor in each electronic fuse is coupled to a second output of the associated high-voltage switch.

16. (Original) A reprogrammable fuse apparatus, comprising:

a plurality of rewriteable electronic fuses arranged in an irregular but predetermined configuration;

a plurality of high-voltage switches, each high-voltage switch corresponding to an associated electronic fuse of said plurality of electronic fuses, and each high-voltage switch having a high-voltage input terminal and at least one fuse-state state-setting input terminal; and

a shift register having an input configured to receive bits of data, said shift register including a plurality of flip-flops, each flip-flop of the plurality of flip-flops having an output terminal coupled to the fuse-state state-setting input terminal(s) of an associated high-voltage switch of the plurality of high-voltage switches.

17. (Original) The reprogrammable fuse apparatus of Claim 16, wherein the rewriteable electronic fuses comprise symmetric serial or parallel fuses.

18. (Original) The reprogrammable fuse apparatus of Claim 16 wherein the rewriteable electronic fuses comprise asymmetric serial or parallel fuses.

19. (Original) The reprogrammable fuse apparatus of Claim 16, wherein each fuse of the plurality of rewriteable electronic fuses comprises:

a latch; and

a nonvolatile memory element coupled to the latch, said nonvolatile memory element configured to be programmed to a memory value capable of causing said latch to settle to a predetermined one of a first state and a second state as a power-up or a reset signal is applied to the fuse.

20. (Original) The reprogrammable fuse apparatus of Claim 19, wherein said latch comprises a MOS latch having two cross-coupled inverters.

21. (Original) The reprogrammable fuse apparatus of Claim 19, wherein said nonvolatile memory element comprises a floating-gate transistor having a floating gate, an amount of charge on the floating gate determining said memory value.

22. (Original) The reprogrammable fuse apparatus of Claim 21, wherein said nonvolatile memory element further comprises a first capacitor having a first plate in common with the floating gate of said floating-gate transistor.

23. (Original) The reprogrammable fuse apparatus of Claim 19, wherein said nonvolatile memory element comprises a nonvolatile memory element manufactured in a MOS process.

24. (Original) The reprogrammable fuse apparatus of Claim 21, wherein said floating-gate transistor is a MOS transistor.

25. (Original) The reprogrammable fuse apparatus of Claim 19, wherein said nonvolatile memory element uses a mechanism selected from the group consisting of: magnetoresistive, ferroelectric, phase-change, and dielectric, for nonvolatile information storage.

26. (Original) The reprogrammable fuse apparatus of Claim 21, wherein the amount of charge on a floating gate may be changed using bidirectional Fowler-Nordheim tunneling.

27. (Original) The reprogrammable fuse apparatus of Claim 21, wherein the amount of charge on a floating gate may be changed using Fowler-Nordheim tunneling.

28. (Original) The reprogrammable fuse apparatus of Claim 21, wherein the amount of charge on a floating gate may be changed using hot-electron injection.

29. (Original) The reprogrammable fuse apparatus of Claim 21, wherein the amount of charge on a floating gate may be changed using direct tunneling.

30. (Original) The reprogrammable fuse apparatus of Claim 21, wherein the amount of charge on a floating gate may be changed using hot-hole injection.

31. (Original) The reprogrammable fuse apparatus of Claim 21, wherein the amount of charge on a floating gate may be changed using ultraviolet radiation exposure.

32. (Original) The reprogrammable fuse apparatus of Claim 22, wherein the nonvolatile memory element further comprises a second capacitor having a first plate in common with the floating gate of said floating-gate transistor.

33. (Original) The reprogrammable fuse apparatus of Claim 19, further comprising a capacitive element coupled to an output of the latch.

34. (Original) The reprogrammable fuse apparatus of claim 21, wherein the latch is predisposed to settle into said first state when a voltage of said floating gate is relatively high and into said second state when the floating-gate voltage is relatively low.

35. (Original) The reprogrammable fuse apparatus of claim 34, further comprising a capacitive element coupled between an output of the latch and a fixed voltage source.

36. (Original) The reprogrammable fuse apparatus of claim 34, wherein said latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a gate-width-to-length ratio that is larger than a gate-width-to-length ratio of at least one of the transistors of a second one of said cross-coupled inverters.

37. (Original) The reprogrammable fuse apparatus of claim 34, wherein said latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a channel doping level that is different from a channel doping level of at least one of the transistors of a second one of said cross-coupled inverters.

38. (Original) An electronic fuse, comprising:

means for providing one of two fuse states; and

means for controlling a memory value coupled to said means for providing, said memory value causing said means for providing to settle to a predetermined fuse state of one of the two fuse states as a power-up or a reset signal is applied to the fuse.

39. (Original) The electronic fuse of Claim 38, wherein the memory value determines to which one of the two fuse states the means for providing settles.

40. (Original) The electronic fuse of Claim 39, wherein the memory value is provided by a rewriteable nonvolatile memory element.

41. (Original) The electronic fuse of Claim 40, wherein said rewriteable nonvolatile memory element comprises a floating-gate transistor.

42. (Original) The electronic fuse of Claim 41, wherein the memory value is determined by an amount of charge stored on a floating gate of the floating-gate transistor.

43. (Original) A reprogrammable fuse apparatus, comprising:

a plurality of rewriteable electronic fuses arranged in an irregular but predetermined configuration;

a plurality of high-voltage switches, each high-voltage switch corresponding to an associated electronic fuse of said plurality of electronic fuses, and each high-voltage switch having a high-voltage input terminal and a fuse-state state-setting input terminal; and

a shift register having an input configured to receive bits of data, said shift register including a plurality of flip-flops, each flip-flop of the plurality of flip-flops having an output terminal coupled to the fuse-state state-setting input terminal of an associated high-voltage switch of the plurality of high-voltage switches.

44. (Original) The reprogrammable fuse apparatus of Claim 43, wherein the rewriteable electronic fuses comprise symmetric serial or parallel fuses.

45. (Original) The reprogrammable fuse apparatus of Claim 43, wherein the rewriteable electronic fuses comprise asymmetric serial or parallel fuses.

46. (Original) The reprogrammable fuse apparatus of Claim 43, wherein each fuse of the plurality of rewriteable electronic fuses comprises:

a latch; and

a nonvolatile memory element coupled to the latch, said nonvolatile memory element configured to be programmed to a memory value capable of causing said latch to settle to a predetermined state as a power-up or a reset signal is applied to the fuse.

47. (Original) The reprogrammable fuse apparatus of Claim 46, wherein said latch comprises a MOS latch having two cross-coupled inverters.

48. (Original) The reprogrammable fuse apparatus of Claim 46, wherein said nonvolatile memory element comprises a floating-gate transistor having a floating gate, an amount of charge on the floating gate determining said memory value.

49. (Original) The reprogrammable fuse apparatus of Claim 48, wherein said nonvolatile memory element further comprises a first capacitor having a first plate in common with the floating gate of said floating-gate transistor.

50. (Original) The reprogrammable fuse apparatus of Claim 46, wherein said nonvolatile memory element comprises a nonvolatile memory element manufactured in a MOS process.

51. (Original) The reprogrammable fuse apparatus of Claim 48, wherein said floating-gate transistor is a MOS transistor.

52. (Original) The reprogrammable fuse apparatus of Claim 46, wherein said nonvolatile memory element uses a mechanism selected from the group consisting of: magnetoresistive, ferroelectric, phase-change, and dielectric, for nonvolatile information storage.

53. (Original) The reprogrammable fuse apparatus of Claim 48, wherein the amount of charge on a floating gate may be changed using bidirectional Fowler-Nordheim tunneling.

54. (Original) The reprogrammable fuse apparatus of Claim 48, wherein the amount of charge on a floating gate may be changed using Fowler-Nordheim tunneling.

55. (Original) The reprogrammable fuse apparatus of Claim 48, wherein the amount of charge on a floating gate may be changed using hot-electron injection.

56. (Original) The reprogrammable fuse apparatus of Claim 48, wherein the amount of charge on a floating gate may be changed using direct tunneling.

57. (Original) The reprogrammable fuse apparatus of Claim 48, wherein the amount of charge on a floating gate may be changed using hot-hole injection.

58. (Original) The reprogrammable fuse apparatus of Claim 48, wherein the amount of charge on a floating gate may be changed using ultraviolet radiation exposure.

59. (Original) The reprogrammable fuse apparatus of Claim 49, wherein the nonvolatile memory element further comprises a second capacitor having a first plate in common with the floating gate of said floating-gate transistor.

60. (Original) The reprogrammable fuse apparatus of Claim 46, further comprising a capacitive element coupled to an output of the latch.

61. (Original) The electronic fuse of claim 48, wherein the latch is predisposed to settle into said first state when a voltage of said floating gate is relatively high and into said second state when the floating-gate voltage is relatively low.

62. (Original) The electronic fuse of claim 61, further comprising a capacitive element coupled between an output of the latch and a fixed voltage source.

63. (Original) The electronic fuse of claim 61, wherein said latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a gate-width-to-length ratio that is larger than a gate-width-to-length ratio of at least one of the transistors of a second one of said cross-coupled inverters.

64. (Original) The electronic fuse of claim 61, wherein said latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a channel doping level that is different from a channel doping level of at least one of the transistors of a second one of said cross-coupled inverters.

65. (Original) A reprogrammable electronic fuse apparatus, comprising:

a plurality of rewriteable electronic fuses arrayed in a predetermined configuration; and

a plurality of high-voltage switches, each high-voltage switch corresponding to an associated electronic fuse of said plurality of electronic fuses, and each high-voltage switch having a high-voltage input terminal and at least one fuse-state state-setting input terminal,

wherein a given electronic fuse of the plurality of electronic fuses is programmed by selecting and coupling an associated control signal to the given electronic fuse.

66. (Original) A reprogrammable electronic fuse apparatus, comprising:

a plurality of rewriteable electronic fuses disposed in an array having a first number of columns and a second number of rows:

a first bus of conductors arranged to supply each electronic fuse with Vdd, Gnd, a high-voltage signal and an intermediate voltage signal;

a program decoder coupled to the first bus of conductors and arranged to receive address information and program data and program an electronic fuse selected by the address information to the state determined by the program data;

a second bus of conductors arranged to control outputs of the electronic fuses;

a readout decoder coupled to the second bus of conductors and arranged to select electronic fuses for reading in response to an address input; and

a plurality of data-out conductors responsive to the readout decoder and the electronic fuses for providing a readout of data stored in the electronic fuses.

67. (Currently Amended) The apparatus of Claim ~~65~~ 66, wherein the first bus of conductors further comprises an initialize conductor for transmitting an initialize signal to the electronic fuses of the array.

68. (Currently Amended) The apparatus of Claim ~~65~~ 66, wherein the plurality of data-out conductors are arranged in columns so that a data-out conductor is coupled to the electronic fuses of a particular column or row.

69. (Original) The apparatus of Claim 68, wherein the data-out conductors are coupled to each electronic fuse through a pass gate controlled by the readout decoder.

70. (Original) The apparatus of Claim 69, wherein there are two complementary data-out conductors coupled to each electronic fuse.

71. (Original) A programmable fuse element for providing one of two fuse states, comprising:

a logic set and reset input;

voltage inputs for ground, Vdd, intermediate-voltage and high-voltage; and

at least one output indicating said output state.

72. (Currently Amended) The programmable fuse element of claim ~~76~~ 71, further comprising an initialize input for initializing the fuse element.

73. (Currently Amended) The programmable fuse element of claim ~~76~~ 71, wherein a magnitude of a signal on the at least one output is [[a]] as large as a magnitude of the high-voltage voltage input and a magnitude of a signal on the set and reset inputs is less than the magnitude of the high-voltage voltage input.